Electric Power Systems Research 80 (2010) 657–666

Contents lists available at ScienceDirect

Electric Power Systems Research

journal homepage: www.elsevier.com/locate/epsr

Power quality improvement using DPC controlled three-phase shunt active filter

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ARTICLE INFO

Article history:
Received 1 October 2007
Received in revised form 26 March 2009
Accepted 25 October 2009
Available online 28 December 2009

Keywords:
Harmonics
Power quality
Active filters
Instantaneous power
Hysteresis comparator
Switching table

ABSTRACT

This paper presents a new control method entitled direct power control (DPC) for shunt active power filter (APF), which is applied to eliminate line current harmonics and compensate reactive power. Its main goal is to rebuild active and reactive source powers to be compared to references values using hysteresis control. The active power reference is issue of DC-side of inverter and reactive power reference is set to zero for unity power factor. The outputs of hysteresis controllers associated with a switching table, control the instantaneous active and reactive power by selecting the optimum switching state of the voltage source inverter (VSI). A theoretical analysis with a complete simulation of the system and experimental results are presented to prove the excellent performance of the proposed technique.

1. Introduction

The generalization of static converters in industrial activities and by consumers leads to an increase in harmonic injection in the network and a lower power factor. These proliferations of non-linear loads result in a deterioration of the quality of voltage waveforms and affect the reliability of power electronic equipments [1,2]. Traditionally, passive LC filters have been used to eliminate lower order harmonics (5th, 7th, 11th . . .) of the line current and then limit the flow of harmonic currents in the distribution system. However, these passive second order filters present many disadvantages such as series and parallel resonances, tuning problems and complexity in the power system, particularly in case of an increase in the number of harmonic components that have to be cancelled [3]. Nowadays, active filters are an interesting alternative to passive filters or in association with hybrid structures [4,5]. For harmonic depollution and reactive power compensation, the most common solution is the three-phase shunt active power filter (APF). This active filter, based on a three-phase voltage source inverter, is connected in parallel with non-linear loads to eliminate current harmonics and compensate reactive power and also to ensure the stability of the system. The performance of the shunt APF depends on the design of the structure, types of controllers and methods used to obtain the reference current [6,7].

In this paper, the control scheme is based on DPC, an approach different from conventional ones, which are based on the instantaneous active and reactive power control loops. In DPC there are not internal current control loops and no PWM modulator bloc, because the converter switching states are selected by a switching table based on the instantaneous errors between the commanded and estimated values of the active and reactive power. Therefore, the key point of the DPC implementation is a correct and fast estimation of the reactive line power.

In general, the converter requires three kinds of sensors as follows: (1) AC current sensors for input current control. (2) A DC-bus voltage sensor for regulating the DC-bus voltage. (3) AC voltage sensors for obtaining the current phase references. The first and the second sensors are absolutely indispensable regarding not only control system, but also system protection, because over current protection of the input lines for the converter is required. The third sensors however can be omitted from the control system loop from the view point of simple implementation. With our approach we develop our control with voltage sensors to calculate active and reactive powers. The three-phase-source currents are measured using only two current sensors. The DC capacitor voltage is regulated and permits to obtain the reference of active power. The IP controller is studied in order to give better performances in time response and system steadiness. The control of the three phases VSI is based on hysteresis comparators associated with a switching table. This solution is simple and owns dynamics and robustness performances. So, in this paper we illustrate the theoretical principles of direct power control with power-source voltage sensors, detail simulation of the above system is analysed, experimental

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doi:10.1016/j.epsr.2009.10.020

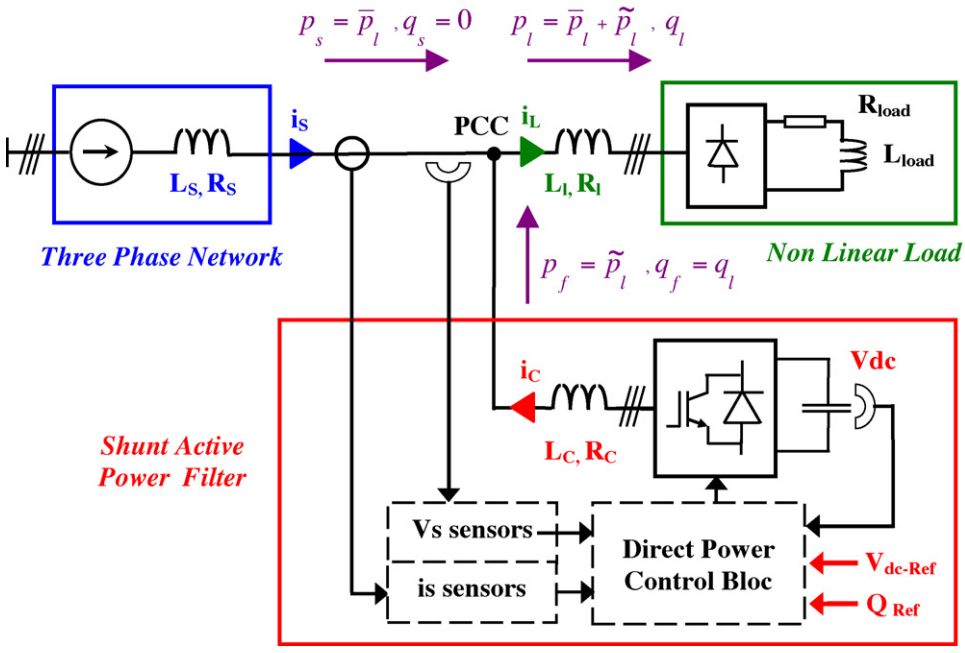

Fig. 1. Shunt active power filter configuration.

results and feasibility of the proposed technique are presented and verified.

2. System configuration and power flow principle

The aim of using this active configuration as shown in Fig. 1 is the compensation of reactive power and elimination of harmonic components. The active filter may be used as a controlled current source and it has to supply a current wave as close as possible to current reference.

In order to generate the current reference, a balance between instantaneous power supplied by the source and the active filter and drained by the load is to be computed. If p_s and q_s are the real and imaginary instantaneous powers supplied by the main while p_f and q_f are the real and imaginary instantaneous power supplied by the active power filter, in order to compensate reactive power and eliminate harmonic currents, the main should supply $p_s = \bar{p}_l$ and $q_s = 0$. The oscillatory component of p_l is to be fed by APF, while q_l must be fully fed by the APF because in this way it is possible to achieve power compensation too. The oscillatory part of p_l is due to harmonic components, so if it is fed to the load by the active filter, source current remains sinusoidal, while the load keeps on receiving the same amount of harmonic and fundamental current. Power balance yields:

$$p_s = \bar{p}_l; \quad q_s = 0 \quad \text{and} \quad p_f = p_l - p_s = \bar{p}_l + \tilde{p}_l - \bar{p}_l = \tilde{p}_l \tag{1}$$

$$q_f = q_l - q_s = q_l \tag{2}$$

Previous Eqs. (1) and (2) need to be modified in order to consider proper operation of the capacitor on the DC side of the inverter. The capacitor stores energy which is utilised as a power supply for the normal operation of the active filter. More in ideal, in normal operating condition APF does not feed active power because it should be able to supply $p_f = \tilde{p}_l$, $q_f = q_l$ and so only reactive power. For this

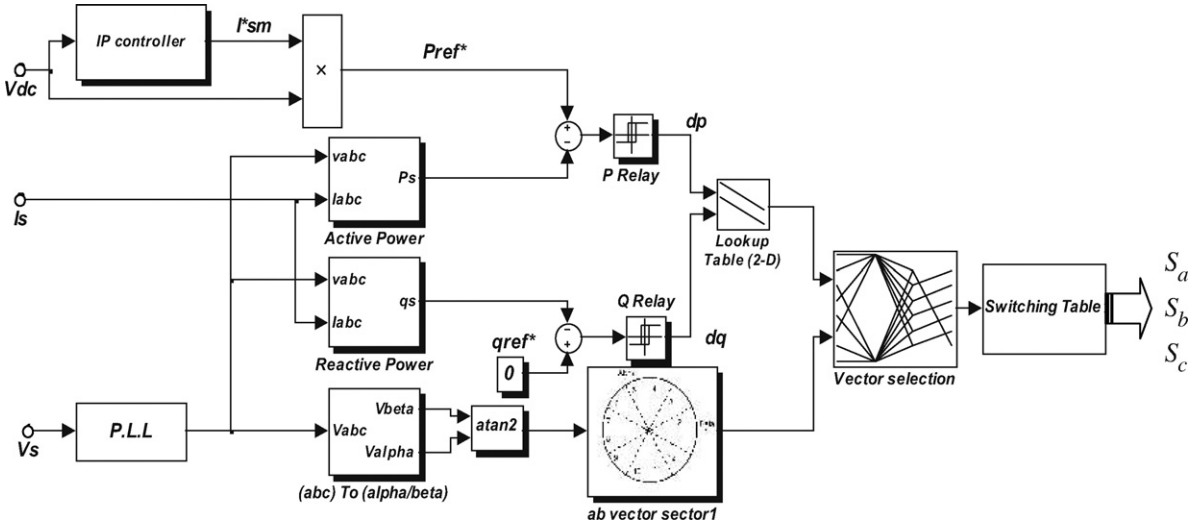

Fig. 2. bloc scheme of DPC with source voltage sensors.

Table 1
The switching table.

d_p	d_q	θ_1	θ_2	θ_3	θ_4	θ_5	θ_6	θ_7	θ_8	θ_9	θ_{10}	θ_{11}	θ_{12}
1	0	101	111	100	000	110	111	010	000	011	111	001	000
	1	111	111	000	000	111	111	000	000	111	111	000	000
0	0	101	100	100	110	110	010	010	011	011	001	001	101
	1	100	110	110	010	010	011	011	001	011	101	101	100

reason, capacitor voltage level is constant during the steady state and varies during transients.

A control of voltage value is needed to regulate voltage level in the steady state and to limit the variability of voltage during transients and during start up. So, the calculation of current reference wave should consider the need to move power balance in order to charge or discharge the DC side capacitor of the active filter. In order to regulate DC voltage level is necessary to control active power balance among source, load and APF. When the load absorbs a precise quantity of power $\bar{p}_l$ and if $p_s > \bar{p}_l$, power in excess is drawn by the APF, which increases DC side voltage. If $p_s < \bar{p}_l$, since the load needs a precise amount of power, the APF feeds the remaining part in order to have $\bar{p}_s + \bar{p}_f = \bar{p}_l$ and so DC voltage level decreases.

3. Direct power control with source voltage sensors

The bloc scheme in Fig. 2 gives the configuration of direct power control where the commands of reactive power q^*_{ref} (set to zero for unity power factor) and active power p^*_{ref} (delivered from the outer integral-proportional (IP) DC voltage controller) are compared with the calculated p_s and q_s values given by (3), in reactive and active power hysteresis controllers, respectively.

$$\begin{aligned} S_s &= p_s + jq_s \\ S_s &= v_{sa}\cdot i_{sa} + v_{sb}\cdot i_{sb} + v_{sc}\cdot i_{sc} \\ &+ j\frac{1}{\sqrt{3}}[(v_{sb}-v_{sc})\cdot i_{sa} + (v_{sc}-v_{sa})\cdot i_{sb} + (v_{sa}-v_{sb})\cdot i_{sc}] \end{aligned} \tag{3}$$

The digitized variables d_p, d_q and the line voltage vector position $\theta_n = arctg(V_{s\alpha}/V_{s\beta})$ form a digital word, which by accessing the address of lookup table selects the appropriate voltage vector according to the switching table. For this purpose, the stationary coordinates are divided into 12 sectors, as shown in Fig. 3, and the sectors can be numerically expressed as:

$$(n-2)\frac{\pi}{6} \le \theta_n \le (n-1)\frac{\pi}{6}, \quad n = 1, 2, \ldots, 12. \tag{4}$$

The digitized error signals d_p, d_q and digitized voltage phase θ_n are input to the switching table in which every switching state, S_a, S_b, and S_c of the converter is stored, as shown in Table 1. By using this switching table, the optimum switching state of the converter can be selected uniquely in every specific moment according to the combination of the digitized input signals. The selection of the optimum switching state is performed so that the power errors can be restricted within the hysteresis bands [8,9].

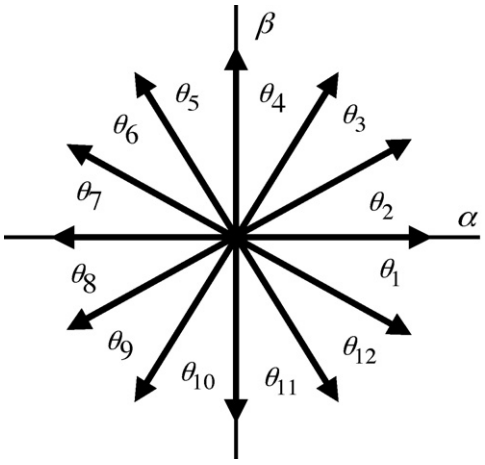

Fig. 3. Sectors on stationary coordinates.

4. Structure of the phase locked loop

Many techniques for P.L.L have been developed, among them the method which detects the zero crossing points of the utility voltages. The drawback with this technique is that these points not only could not be exactly detected if the signal contains high frequency perturbation (HF), but also they can be detected only at every half-cycle of the utility period. Then, the phase tracking is impossible between the detected points, and fast tracking performance cannot be achieved.

The second method is to use the quadrate of the signal [10] for the determination of the amplitude and phase or angular position.

The P.L.L. allows controlling an estimated phase angle $\hat{\theta} = \omega \cdot t$ with respect of the utility phase angle $\theta = \omega \cdot t$. The system voltages are converted to the α-β coordinates system by the Concordia transformation as:

$$\begin{bmatrix} v_{s\alpha}(\theta) \\ v_{s\beta}(\theta) \end{bmatrix} = [T_{32}]^t \cdot \begin{bmatrix} v_{sa}(\theta) \\ v_{sb}(\theta) \\ v_{sc}(\theta) \end{bmatrix} \tag{5}$$

The d–q voltage components are derived by the park's transformation where $\hat{\theta}$ represents the instantaneous reference voltage vector angle:

$$\begin{bmatrix} v_{sd} \\ v_{sq} \end{bmatrix} = P(\hat{\theta}) \cdot \begin{bmatrix} v_{s\beta}(\theta) \\ v_{s\alpha}(\theta) \end{bmatrix} \quad \text{with } P(\hat{\theta}) = \begin{bmatrix} \cos\hat{\theta} & \sin\hat{\theta} \\ -\sin\hat{\theta} & \cos\hat{\theta} \end{bmatrix} \tag{6}$$

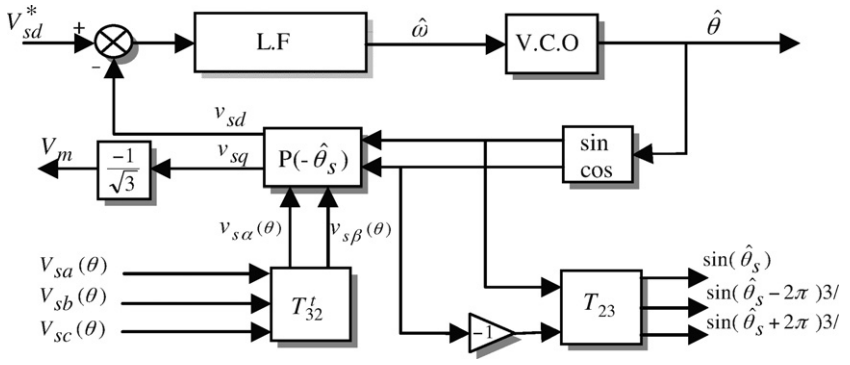

Fig. 4. Detail bloc diagram of P.L.L.

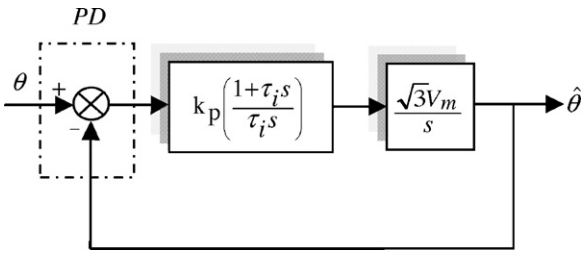

Fig. 5. Simplified model for P.L.L.

Substituting (5) in (6) the voltages v_{sd} and v_{sq} are given by:

$$\begin{bmatrix} v_{sd} \\ v_{sq} \end{bmatrix} = \sqrt{3} \cdot V_m \cdot \begin{bmatrix} \sin(\theta - \hat{\theta}) \\ -\cos(\theta - \hat{\theta}) \end{bmatrix} \tag{7}$$

where, V_m is the source voltage amplitude.

Assume that the phase angle $(\theta - \hat{\theta})$ is small then from (7) one can write:

$$v_{sd} = \sqrt{3} \cdot V_m(\theta - \hat{\theta}) \tag{8}$$

The P.L.L will be locked onto the supply voltage when the error $\Delta\theta = \theta - \hat{\theta}$ is set to zero. In this case $v_{sd} = 0$ and $v_{sq} = -\sqrt{3} \cdot V_m$. So, it is possible to control θ by regulating v_{sd} to zero.

Fig. 4 represents the basic form of the P.L.L, a negative feedback control loop comprising a phase detector (PD), a loop filter (LF) and a voltage controlled oscillator (VCO). The angular frequency, $\hat{\omega}$ is given by:

$$\hat{\omega} = \frac{d\hat{\theta}}{dt} = F_{LF}(s)\sqrt{3} \cdot V_m \cdot (\theta - \hat{\theta}) \tag{9}$$

Here $F_{LF}(S)$ denotes the loop filter, which is expressed in this case by the following transfer function:

$$F_{LF}(s) = k_p + \frac{k_i}{s} = k_p \left(\frac{1 + \tau_i s}{\tau_i s} \right) \tag{10}$$

Then the angular position $\hat{\theta}$, the output of VCO, will be:

$$\hat{\theta} = \frac{1}{s}\hat{\omega} \tag{11}$$

Fig. 4 can be simplified and becomes similar to Fig. 5.The closed loop transfer function of this system is given by:

$$\frac{\hat{\theta}(s)}{\theta(s)} = \frac{\sqrt{3}V_m k_p(1 + \tau_i s/\tau_i s)(1/s)}{1 + \sqrt{3}V_m k_p(1 + \tau_i s/\tau_i s)(1/s)} \tag{12}$$

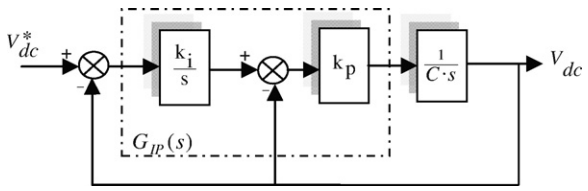

Fig. 7. Control closed loop of DC voltage.

Identify the transfer function with the general second order defined by:

$$F(s) = \frac{2\xi\omega_n s + \omega^2}{s^2 + 2\xi\omega_n s + \omega_n^2} \tag{13}$$

Allows determining the parameters of $F_{LF}(S)$:

$$k_p = \frac{2\xi\omega_n}{\sqrt{3}V_m} \quad \text{and} \quad \tau_i = \frac{2\xi}{\omega_n} \tag{14}$$

In order to realize a good trade-off between stability and dynamic performance, one can choose $\xi = 0.707$ and $f_n = \omega_n/2\pi = 50$[Hz] then: $k_p = 1.07$ and $\tau_i = 4.5 \times 10^{-3}$[s].

The P.L.L simulation in Fig. 6 is done with signal containing harmonics and random noise (HF):

$$V_{sa} = 50\sqrt{2}\sin(\omega t) + \frac{50\sqrt{2}}{5}\sin(5\omega t) + \frac{50\sqrt{2}}{7}\sin(7\omega t) + Noise[-100, 100] \tag{15}$$

One can clearly see the compromise between the response time and the quality of signals, which is strictly related to the choice of the L.F.

5. DC voltage IP controller

To reduce the DC-link capacitor fluctuation voltages and compensate the system loss, an integral-proportional controller $G_{IP}(S)$ is used in the DC-link voltage control loop.

At high operating switching frequency, the inner instantaneous power control must be much faster, which means that p_s, q_s follow p^*_{ref}, q^*_{ref} respectively. Hence, we can assume that a closed loop powers controller transfer function will be equal to unity $G_{p,q}(S) = 1$.Therefore; the choice of IP parameters (k_i, k_p) is based on step response of the closed loop shown in Fig. 7.

$$\frac{V_{dc}}{V^*_{dc}} = \frac{k_p \cdot k_i/C}{s^2 + k_p/C \cdot s + k_p \cdot k_i/C} \tag{16}$$

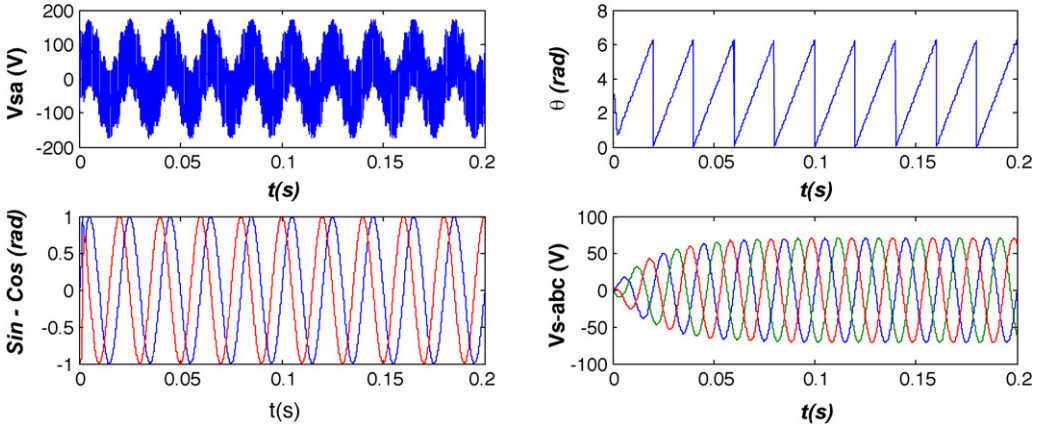

Fig. 6. P.L.L simulation results.

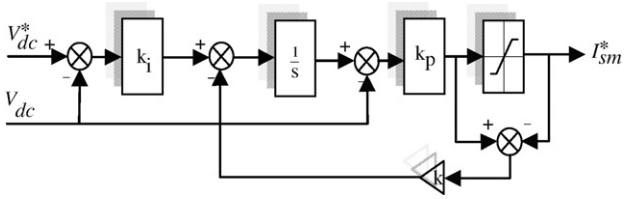

Fig. 8. An anti-windup IP controller system.

From (16) the relation between V_{dc} and V^*_{dc} is a second order transfer function (TF) [11]:

$$\frac{V_{dc}}{V^*_{dc}} = \frac{\omega^2}{s^2 + 2\xi\omega_n s + \omega_n} \tag{17}$$

where, ω_n ξ are the natural frequency and the damping coefficient respectively. The TF contains two poles and does not possess a zero; this proves that the IP controller insures a fast response and a good stability for transient states relatively to the PI controller.

By equaling (16) and (17):

$$\frac{k_i k_p}{C} = \omega_n^2 \quad \text{and} \quad \frac{k_p}{C} = 2\xi\omega_n.$$

Hence,

$$k_p = 2\xi\omega_n C \quad \text{and} \quad k_i = \frac{\omega_n}{2\xi}$$

Finally, to limit and smooth mains current at starting and dumping transient time, we have introduced additionally to the IP controller an anti-windup compensation, to deal with the adverse effects caused by control saturation shown in Fig. 8.

6. Modelling and simulation of the system

To simulate the D.P.C of the shunt APF, a model in MATLAB\SIMULINK® and SimPower-Systems Bloc set is developed. The complete active filter is composed mainly of a three-phase source, a non-linear load (Rectifier & R, L), a PWM VSI, and D.P.C controller. The same experimental test bench parameters are used

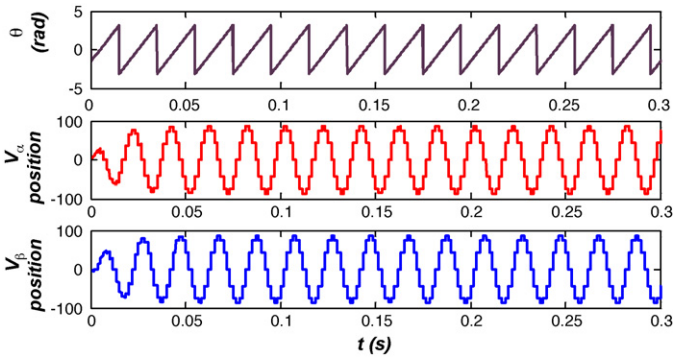

Fig. 9. Instantaneous angle, α-β frame voltage position.

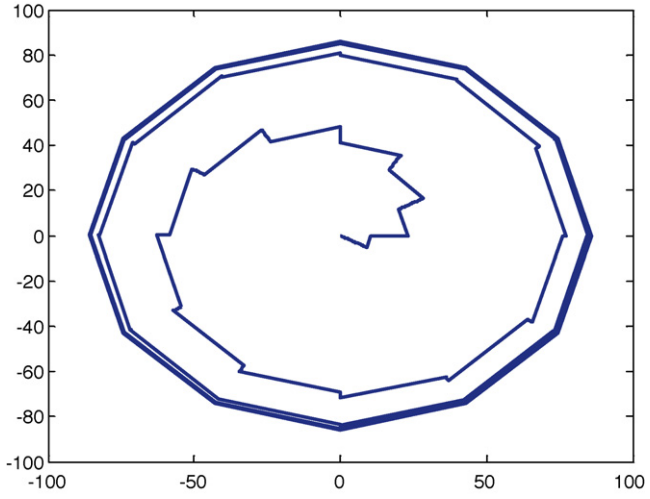

Fig. 10. Source vector evolution.

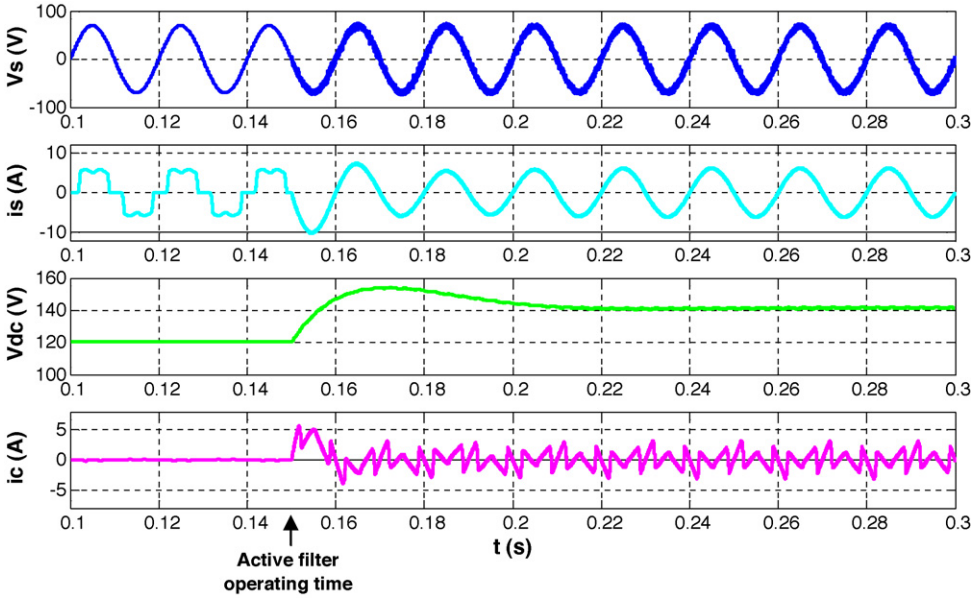

Fig. 11. Source voltage, source current, DC side capacitor voltage and filter current waveforms. Filter switched on at 0.15 s.

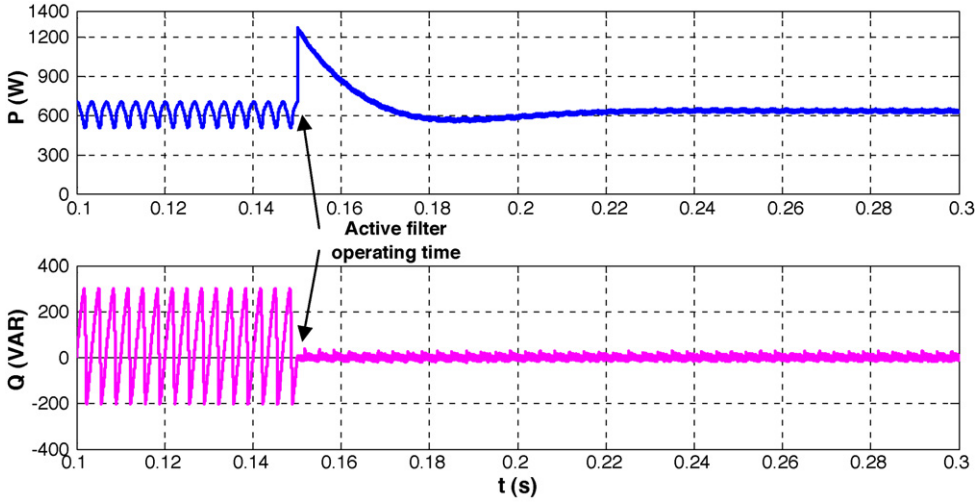

Fig. 12. Active and reactive powers source. Filter switched on at 0.15 s.

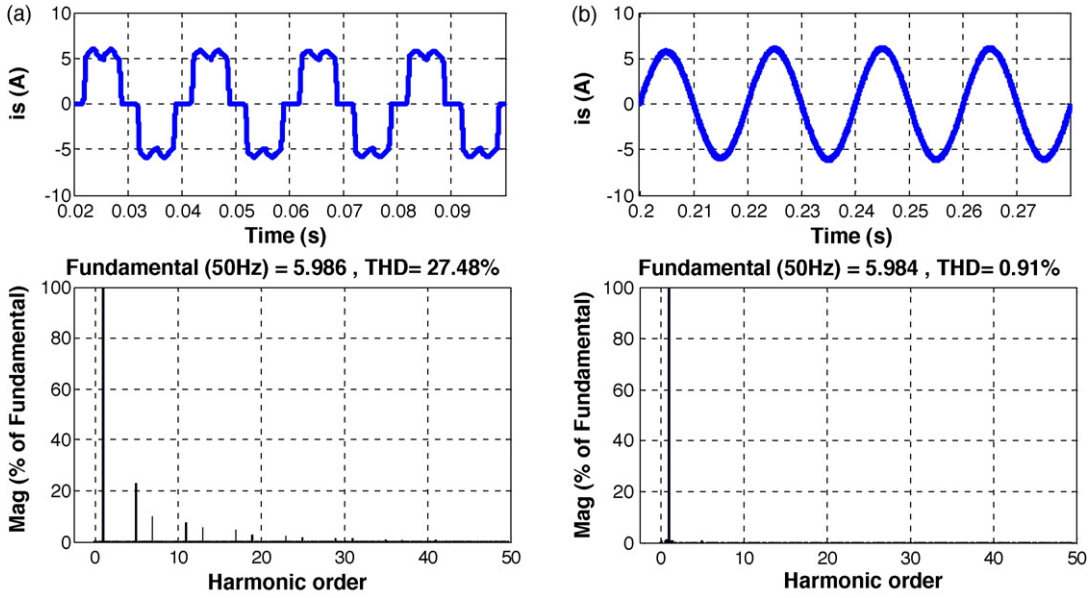

Fig. 13. Source current and its spectrum: (a) before filtering and (b) after filtering.

for simulation:

$V_s = 50\,\mathrm{V}(rms)$, $R_s = 0.1\,\Omega$, $L_s = 0.1\,\mathrm{mH}$, $R_c = 0.01\,\Omega$, $L_c = 1\,\mathrm{mH}$,
$R_l = 0.01\,\Omega$, $L_l = 0.566\,\mathrm{mH}$, $R_{L1} = 21\,\Omega$ and $R_{L2} = 10\Omega$, $L_L = 1\,mH$,
$V_{dc}^{*} = 142\,\mathrm{V}$, $C = 1100\,\mu\mathrm{F}$, $HB_P = HB_Q(hysteresis\,band) = 0.1$, $K_i = 54.55$ and $K_p = 0.12$.

On the one hand Figs. 9 and 10 illustrate the evolution of the source vector on the two axes α-β, its angle θ and its representation in the polar coordinates. On the other hand and firstly; to study the performance of the proposed APF control, first simulation is carried out with a fixed load and the APF is switched on at 0.15 s. Fig. 11 shows the source voltage (V_{sa}), source current (i_{sa}), dc side capacitor voltage (V_{dc}) and filter current (i_{ca}). The filter is switched on at 0.15 s. The instant the filter is switched on the source current becomes sinusoidal from the stepped wave shape, and capacitor voltage reaches a steady-state value within a few cycles. In Fig. 12 one can see that the active power joined its nominal value and that reactive energy becomes null when the active filter is activated at this moment.

Fig. 13 shows the source current spectrum analysis before and after filtering. Before filtering; one can see the current harmonics distortion value was $THD_i = 27.48\%$ and after filtering it will be $THD_i = 0.91\%$.

Secondly, to show the performance during transient condition the load current is changed at 0.3 s. Figs. 14 and 15 show the various waveforms during load change. When the load current is increased (reduced), capacitor voltage decreases (increases) to compensate for the real power supplied by the source. The dynamic performance of the designed IP controller is found to be satisfactory, and the steady-state condition is reached within 3–4 cycles of the ac mains.

7. Experimental results

The APF experimental test bench used was developed in LAII-ESIP laboratory (Fig. 16a). The control strategy is implemented

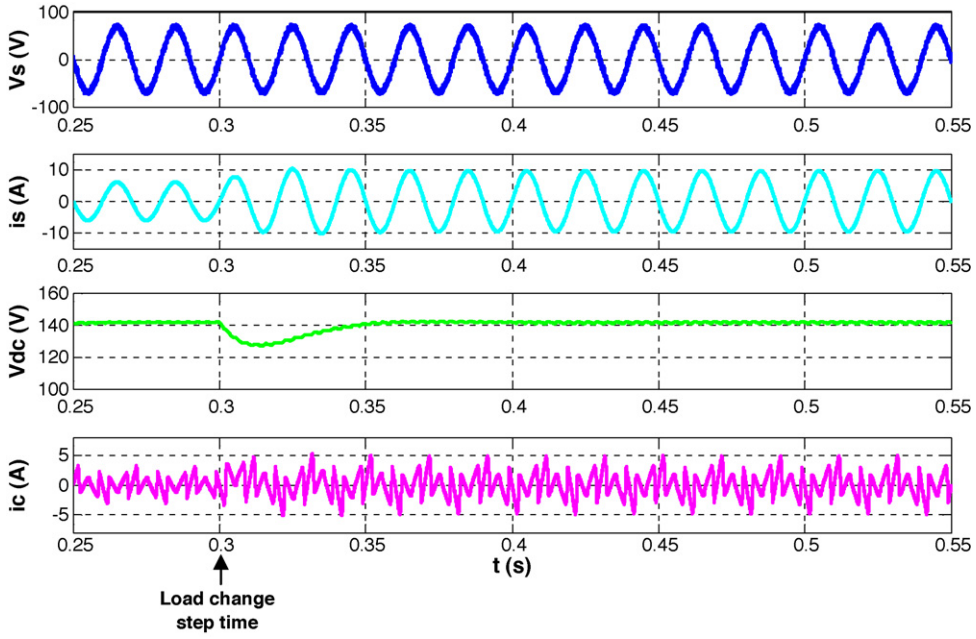

Fig. 14. Source voltage, source current, DC side capacitor voltage and filter current waveforms. Load change at 0.3 s.

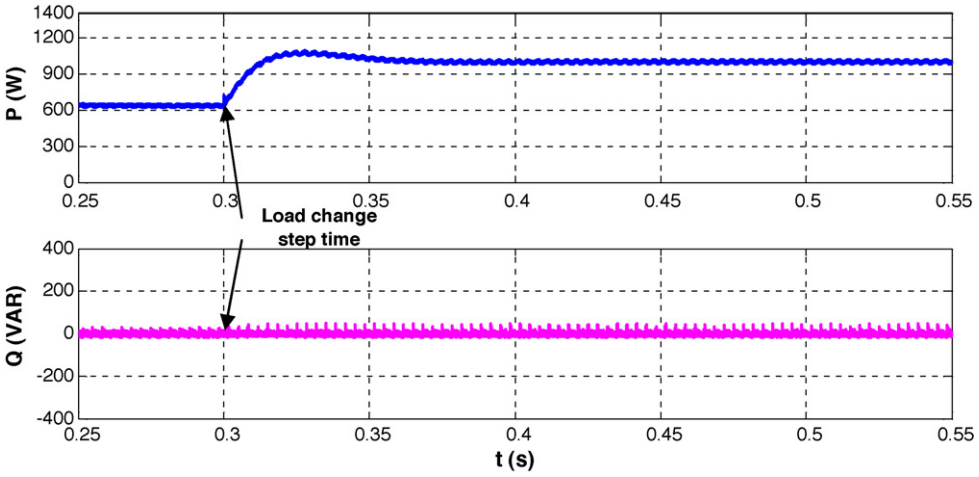

Fig. 15. Active and reactive powers source. Load change at 0.15 s.

(a) Shunt active power filter (b) Real-time system implementation

Fig. 16. Laboratory test bench. (a) Shunt active power filter; (b) real-time system implementation.

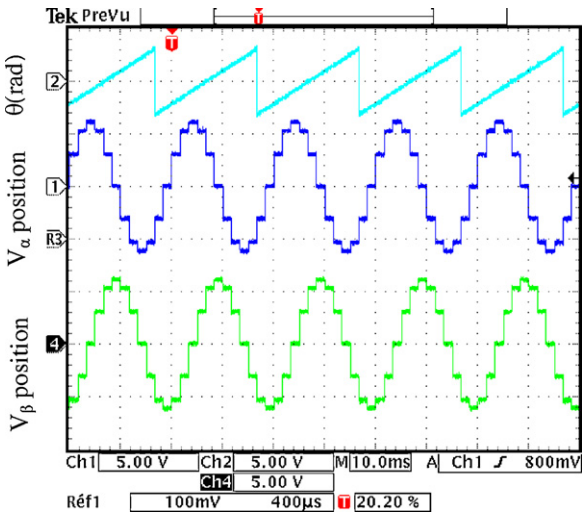

Fig. 17. Instantaneous angle, α-β frame voltage position.

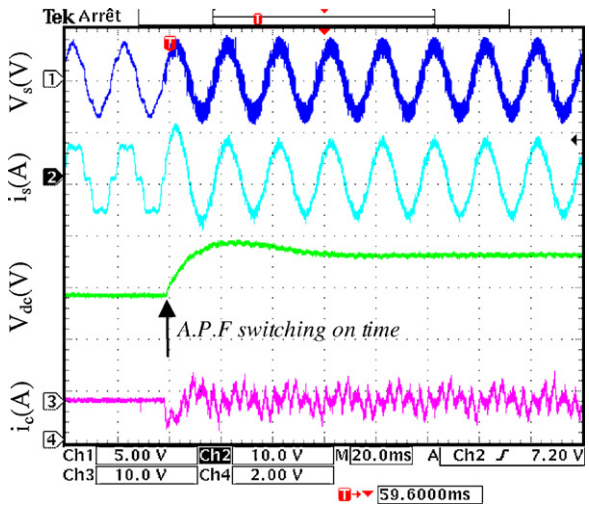

Fig. 19. Source voltage, source current, DC side capacitor voltage and filter current waveforms, filter switched on.

using a single-board DS1104 manufactured by dSPACE company and developed under the integrated development environment of MATLAB-SIMULINK RTW provided by The MathWorks, inc (Fig. 16b). The sampling time using in practical tests for the proposed system is 100 µs, and experimental results are obtained with the same parameters used in simulation.

Fig. 17 shows practically again that P.L.L provides also a good estimation of θ, and then generates good sine and cosine voltage position when the input voltages contain harmonics and HF noise. In Fig. 18 it illustrates the evolution of VSI voltage vector in the 12 sectors by selecting the optimum switching state. It can be noticed in Fig. 19 that as soon as the filter is switched on it starts injecting harmonic current into the line. Steady state is reached with the build-up of dc bus capacitor voltage, and the supply current becomes sinusoidal from the stepped wave shape, by consequence the instantaneous active power continues following its reference and reactive power will be null (Fig. 20). The response during a change of load is shown in Figs. 21 and 22, it is noticeable that for a change in load there is smooth change in the source current from $Is = 4.3$ to $Is = 8.8$ A and capacitor voltage decreases from the reference value to deliver the energy during the transient period. However; in this condition the active power steps from $P = 648$

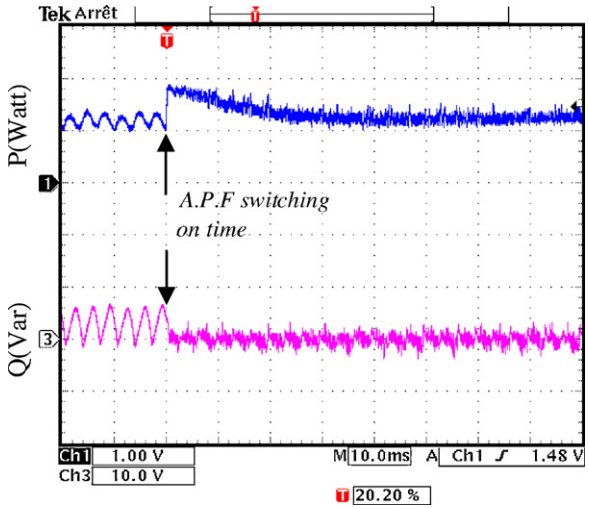

Fig. 20. Active and reactive powers source, filter switched on.

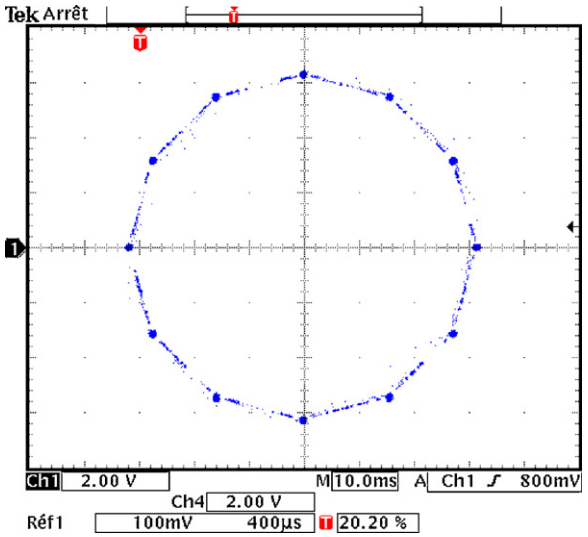

Fig. 18. Source vector evolution.

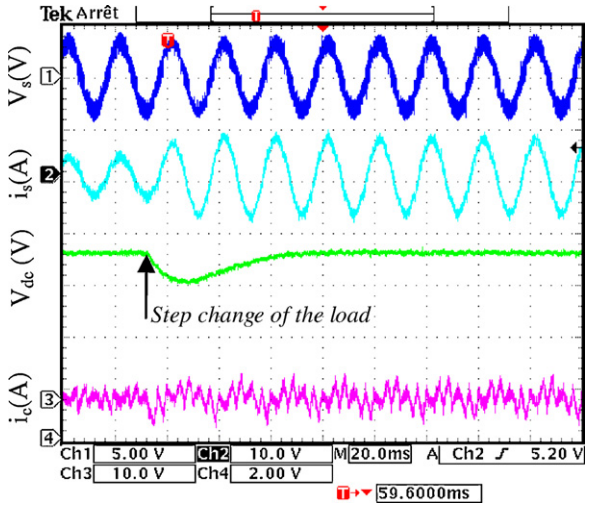

Fig. 21. Source voltage, source current, DC side capacitor voltage and filter current waveforms, step load change.

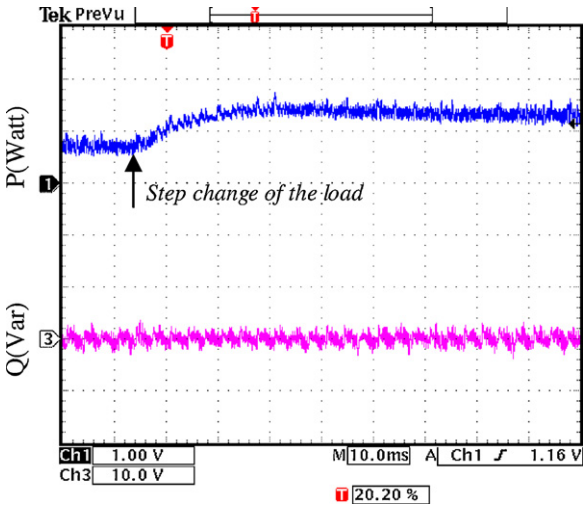

Fig. 22. Active and reactive powers source, step load change.

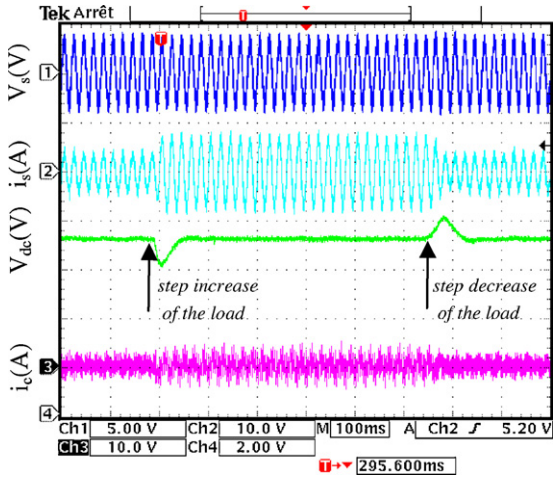

Fig. 23. Step on/down change of the load: source voltage, source current, DC side voltage and filter current evolution.

to $P = 1317$ W relatively to the load need, on the other hand reactive power does not change, and still follows its null reference. In Figs. 23 and 24 one can see the robustness of the control with double changes in the load. Figs. 25 and 26 show the spectrum analysis

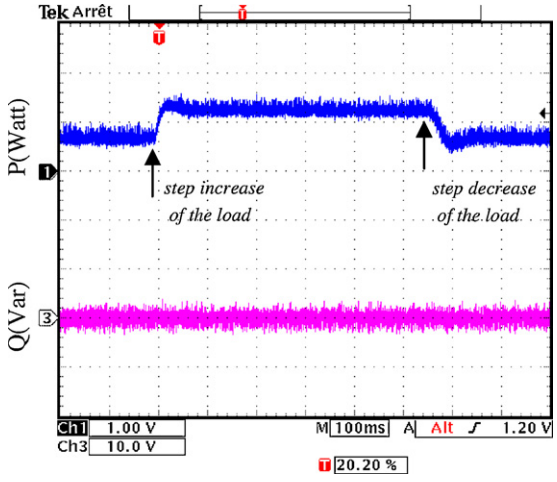

Fig. 24. step on/down change of the load: active and reactive powers evolution.

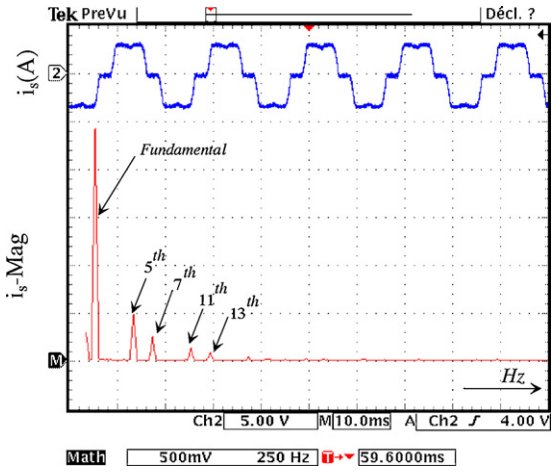

Fig. 25. Source current and its spectrum before filtering.

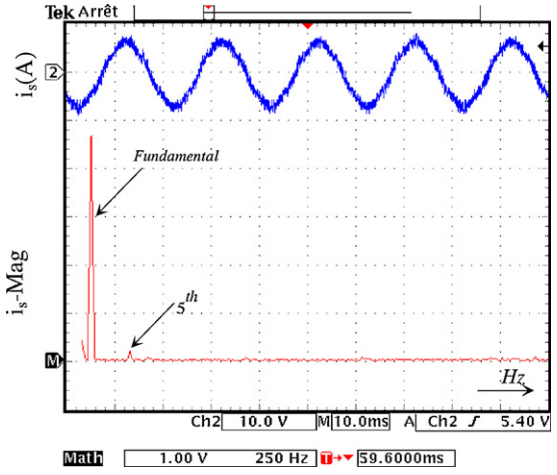

Fig. 26. Source current and its spectrum after filtering.

of the main current before compensation when the $THD_i = 23.4\%$ and after compensation $THD_i = 5.5\%$.

8. Conclusion

A DPC for shunt APF has been presented. One can see that the control algorithm is simple, decoupling between active and reactive current is not required, there is no current regulation loops, it has a good dynamics, and it offers sinusoidal line currents (low THD) for ideal and distorted line voltage and compensates automatically the reactive power part to improve the main power factor to unity. The experimental results on real test bench of laboratory prove that one can improve quality (shattering) of the signals with decreasing sample time more than 10^{-4} s by changing the hard platform (DSP) or introducing SVM technique to obtain a constant switching. Moreover, this new control method is easy to be calculated and implemented. Also, the control strategies can be improved by using sensorless source voltage techniques and be tested for tensions and more important powers.

Appendix A. List of symbols

DPC	direct power control
APF	active power filtering
VSI	voltage source inverter

PWM	pulse width modulation
IP	integral-proportional
DC	continuous
PLL	phase locked loop
VCO	voltage controlled oscillator
PD	phase detector
LF	loop filter
TF	transfer function
THD	total harmonic distortion
L_s	source internal inductance
R_s	source internal resistance
L_c	APF filter inductance
R_c	APF filter resistance
L_l	serie load inductance
R_l	serie load resistance
v_{si}	($i = a,b,c$) source voltages in reference a,b,c frame
v_{sc}	($c = \alpha,\beta$) source voltages in Concordia coordinates
v_{sp}	($p = d,q$) source voltages in Park transformation
p	instantaneous real power
$\bar{p}$	average real power
$\tilde{p}$	oscillating part of real power
q	instantaneous imaginary power
$\bar{q}$	average imaginary power
$\tilde{q}$	oscillating part of imaginary power

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