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Design of low power CMOS ultra wide band low noise amplifier using noise canceling technique

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ABSTRACT

This paper presents a design of a low power CMOS ultra-wideband (UWB) low noise amplifier (LNA) using a noise canceling technique with the TSMC 0.18 μm RF CMOS process. The proposed UWB LNA employs a current-reused structure to decrease the total power consumption instead of using a cascade stage. This structure spends the same DC current for operating two transistors simultaneously. The stagger-tuning technique, which was reported to achieve gain flatness in the required frequency, was adopted to have low and high resonance frequency points over the entire bandwidth from 3.1 to 10.6 GHz. The resonance points were set in 3 GHz and 10 GHz to provide enough gain flatness and return loss. In addition, the noise canceling technique was used to cancel the dominant noise source, which is generated by the first transistor. The simulation results show a flat gain (S_{21} > 10 dB) with a good input impedance matching less than −10 dB and a minimum noise figure of 2.9 dB over the entire band. The proposed UWB LNA consumed 15.2 mW from a 1.8 V power supply.

1. Introduction

Recently, the ultra wideband (UWB) systems have become popular wireless communication applications. Since the Federal Communications Commission (FCC) released the 7.5 GHz bandwidth of the spectrum range from 3.1 to 10.6 GHz for ultra wideband in 2002 [1]. As the essential reasons to use UWB systems, it provides a low power level (limit to −41.3 dBm/MHz) and high data-rate (up to 480 Mb/s) for wireless communications. The UWB low noise amplifier (LNA) has several requirements, such as sufficient wideband in/output return loss, sufficient flat gain over the entire 7.5 GHz bandwidth, low noise figure for sensitivity, low power consumption for mobility, and a small chip area for low cost.

Traditionally, UWB LNA has been approached to overcome the enormous bandwidth. The distributed amplifier provides wide bandwidth characteristics, good linearity and sufficient in/output matching conditions [2,3]. On the other hand, it consumes a large DC current to operate multi-amplifying stages and occupies a significant chip area. The resistive shunt-feedback amplifier is used for UWB LNA [4], which has a few hundred of feedback resistors to extend the bandwidth. On the other hand, it tends to degrade the noise performance because of the feedback resistor peak near the input stage. The passive filter was also adopted for designing the UWB LNA [5]. It provides a wide input matching characteristic. On the other hand, it requires some passive components, such as an inductor, which requires a large chip size. The common-gate stage at the 1st topology is currently used to design a wideband amplifier due to the constant wideband input impedance of $1/g_m$ [6]. On the other hand, the common-gate stage suffers from poor noise performance. For this reason, the noise canceling technique has been implemented with the common-gate stage [7–10], but it also has large power consumption to obtain low noise, sufficient gain, and wideband matching characteristics.

To solve this problem, a low power noise-canceling UWB LNA is proposed. It consists of a common-gate stage at the 1st stage for wideband input matching, a current-reused structure to save power dissipation compared to the previous reported noise-canceling UWB LNAs [11], and a stagger tuning structure for flat gain using inter-stage matching. Furthermore, the output buffer was employed for the measurements using the source-follower.

The paper is organized as follows. In Section 2, the proposed UWB low noise amplifier is described to validate the theory and technique for low power and noise performance. Section 3 reports the simulation results of gain, reflection coefficient, reverse isolation, noise figure and IIP3 in the entire band. The performances of the proposed UWB LNA are compared with the previously proposed UWB LNAs. Section 4 presents the conclusion.

2. Design of UWB LNA

Fig. 1 shows a schematic diagram of the proposed UWB LNA. This proposed circuit consists of a common-gate topology at the

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input stage for wide input impedance matching characteristics, a noise canceling structure to reduce the dominant noise source from M_1, a cascode current-reused structure for low power consumption [12], and an output buffer. In addition, the series-inductor peaking was employed for bandwidth extension at the output stage [13]. The design concepts of the LNA are detailed as follows.

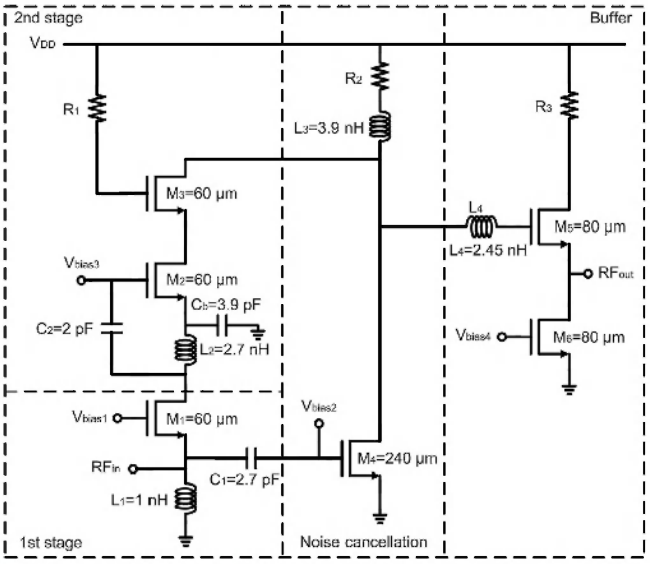

Fig. 1. Schematic diagram of the proposed UWB LNA. V_{DD} is a 1.8 V supply voltage. V_{bias1}, V_{bias2}, and V_{bias3} are the biasing voltage for the common-gate stage M_1, cascode stage M_2 and M_3, and M_4.

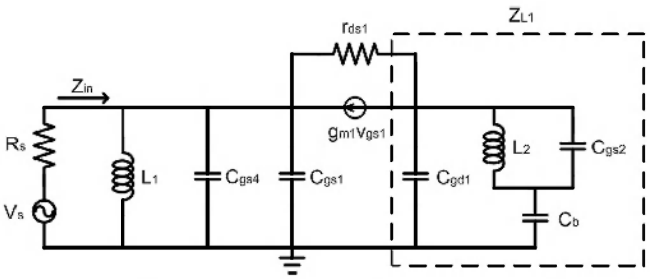

Fig. 2. Small signal equivalent circuit for calculating the input impedance (Z_{in}) of the input stage network in Fig. 1.

2.1. Wide input matching using a common-gate stage

Conventionally, the common-gate stage is well known for a wide-band input matching of $1/g_{m1}$, even though it has poorer noise performance than the common-source stage. The common-gate stage has become a useful component instead of the common-source stage at the high frequency area [6]. The common-gate stage has an advantage in size compared to the common-source stage, which needs some passive components, such as a resistive shunt feedback topology and band pass filter for a wide band input impedance matching to design UWB LNA.

This study is considered as a Q-factor to achieve wide band input impedance matching. The lower Q-factor results in a wider bandwidth considering the parasitic capacitance in gate and source [14], the Q-factor of the common-source and common-gate stages can be derived as follows:

$$Q_{CS} = \frac{1}{2\omega C_{gs} R_s} \tag{1}$$

$$Q_{CG} = \frac{\omega C_{gs} R_s}{2} \tag{2}$$

where C_{gs} is the parasitic gate to source capacitance and R_s is the source resistance. The common-gate stage has low Q-factor, and then it provides a broadband input matching characteristic easily. Therefore, the common-gate stage can provide a small chip area by eliminating input passive elements which require more chip area for broadband matching. Fig. 2 shows the small-signal equivalent circuit for the input stage. The input impedance Z_{in} of the proposed circuit can be derived as follows:

$$Z_{in}(s) = \frac{1}{g_{m1} + \frac{1}{Z_S(s)} + \frac{1 - g_{m1} Z_{L1}(s)}{r_{ds1} + Z_{L1}(s)}}$$

$$Z_S(s) = sL_1 // \frac{1}{sC_{gs1}} // \frac{1}{sC_{gs4}}$$

$$Z_{L1}(s) = \frac{1}{sC_{gd1}} // \left[(sL_2 // \frac{1}{sC_{gs2}}) + \frac{1}{sC_b} \right] \tag{3}$$

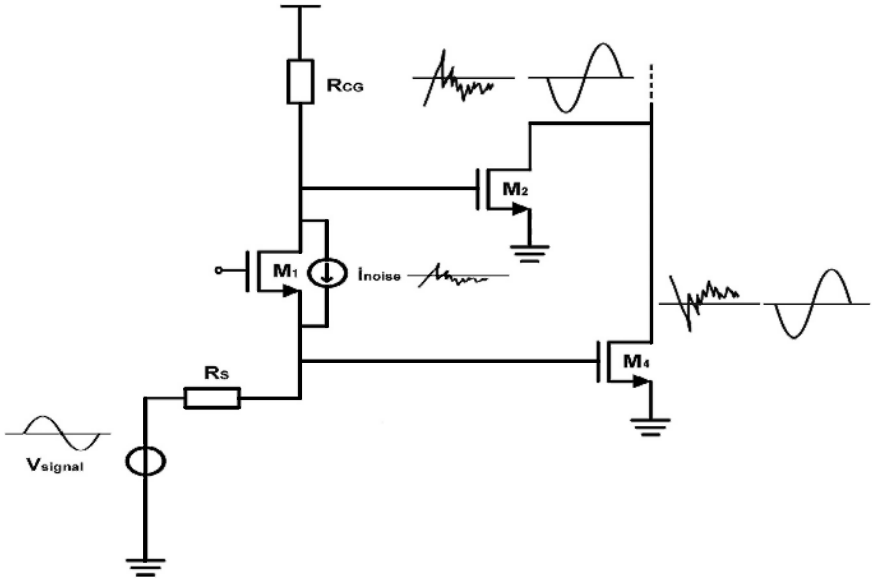

Fig. 3. Principle of noise canceling technique used as a common-gate to generate the anti-phase of noise source at drain and source using voltage variation. –Av is made by common-source stage, $M4$.

where g_{m1} is the transconductance of M_1, L_1 is the RF (Radio Frequency) choke, C_{gs1} is the parasitic capacitance of M_1, and C_{gs4} is the parasitic capacitance of M_4. These four components are important sources to obtain a wideband input impedance matching condition.

2.2. Noise canceling principle

The purpose of noise canceling technique is to decouple the input matching with the NF. Noise is generated mainly by the first transistor, which is the common-gate stage M_1 in Fig. 1. The noise canceling technique was used to reduce the dominant noise source. Fig. 3 represents the noise canceling technique conceptually assuming that the input impedance is well matched to $1/g_m$ ($=50\ \Omega$). The noise current (i_{noise}) flows via R_s to ground, where generates a voltage variation at the source of M_1. This noise current also flows via R_{CG}, which occurs in a voltage variation at the drain of M_1. Therefore, it creates two fully correlated noise voltages at the drain and source. The noise current can be canceled in the proposed circuit using these correlated noise voltages. By properly designing g_{m2} and g_{m4}, the noise contributed by M_1 can be canceled at the output. The noise current due to M_1 can be derived by the following [7]:

$$I_{n\,out} - \frac{I_{n,M1}}{1+g_{m1}R_s}(g_{m2}R_{CG}-g_{m4}R_s) \tag{4}$$

Based on Eq. (4), the sufficient condition of noise canceling can be expressed as follows:

$$g_{m2}R_{CG} = g_{m4}R_s \tag{5}$$

After noise canceling, the dominant noise is generated by transistors M_2 and M_3. The noise factor can be approximated as follows:

$$F = 1 + \frac{R_s}{R_{CG}} + \frac{R_s}{R_{CG}}\frac{\gamma}{\alpha}\frac{1}{g_{m2}R_{CG}} + \frac{\gamma}{\alpha}\frac{1}{g_{m4}R_s} \tag{6}$$

where $\alpha = g_m/g_{d0}$, g_{d0} is the channel conductance for $V_{DS}=0$ and γ is the noise parameter. In addition, the common-source stage, M_2 and M_4, were adopted to increase the wanted signal and noise voltage. In particular, the size of transistor M_4 was designed to consider the ratio of transistor M_1 [9]. To determine the optimized ratio of the transistors, Fig. 4 represents the extensive simulation results of the noise imbalance from the two different paths, which provides the anti-phase of noise and generates at the source and drain of the common-gate stage, M_1. As shown in Fig. 4, noise impedance is simulated at the drains of M_3 and M_4 before combining the total noise. Therefore, the well matched point for noise canceling is near the zero value at low frequency. Indeed, the minimum noise figure was obtained near the zero value. As a result, M_1 was chosen to be 60 μm and M_4 was four times larger than M_1.

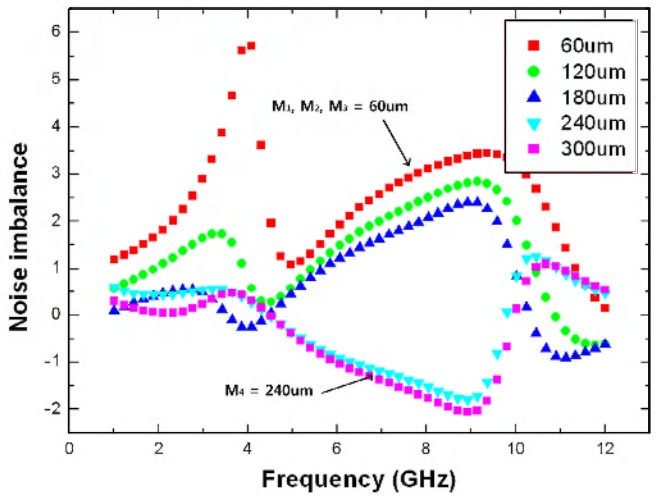

Fig. 4. Extensive simulation results of the noise imbalance with regard to the variation in size of transistor *M4*. The gate lengths were varied to 60 μm, 120 μm, 180 μm, 240 μm and 300 μm.

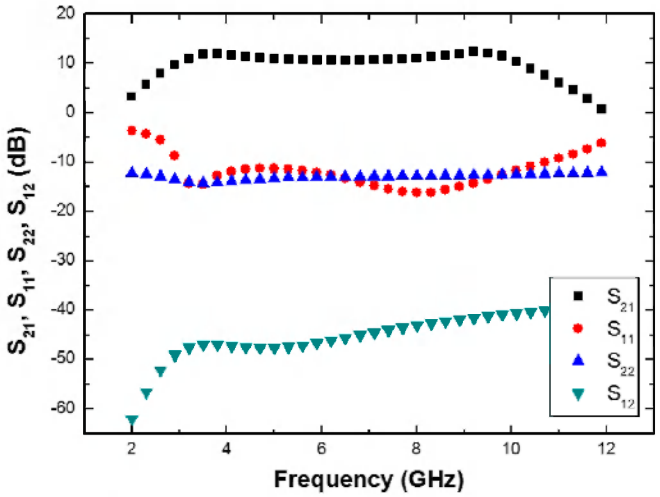

Fig. 6. Calculated frequency responses of voltage gain (S_{21}), input return loss (S_{11}), output return loss (S_{22}), and reverse isolation (S_{12}) as a function of frequency.

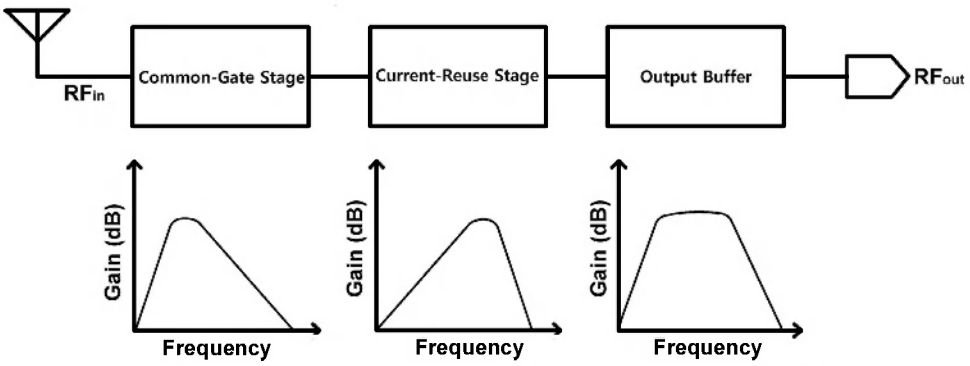

Fig. 5. Block diagram of the stagger tuning technique for inter-stage matching using the low frequency band (3 GHz) and high frequency band (10 GHz).

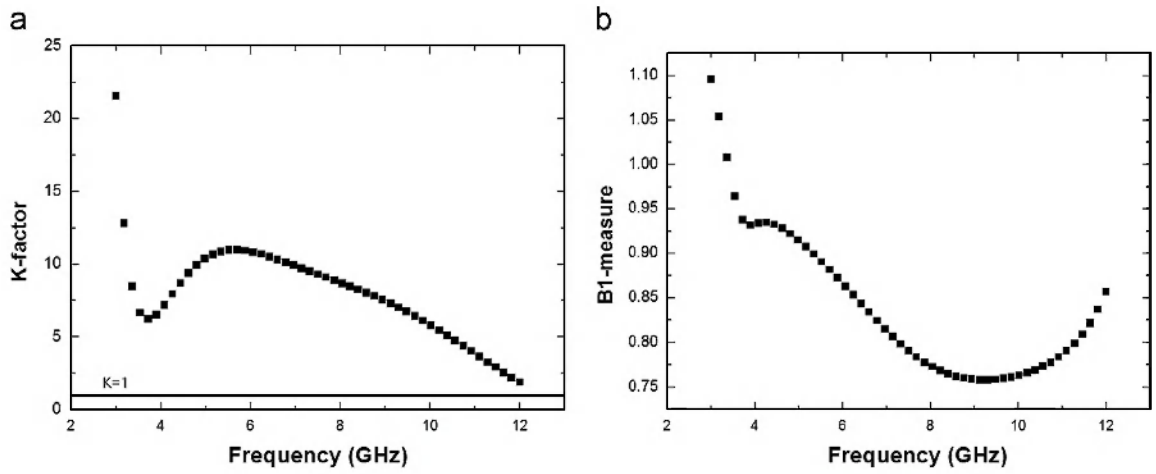

Fig. 7. (a) *K*-factor and (b) *B*1-measure of the proposed UWB LNA versus frequency.

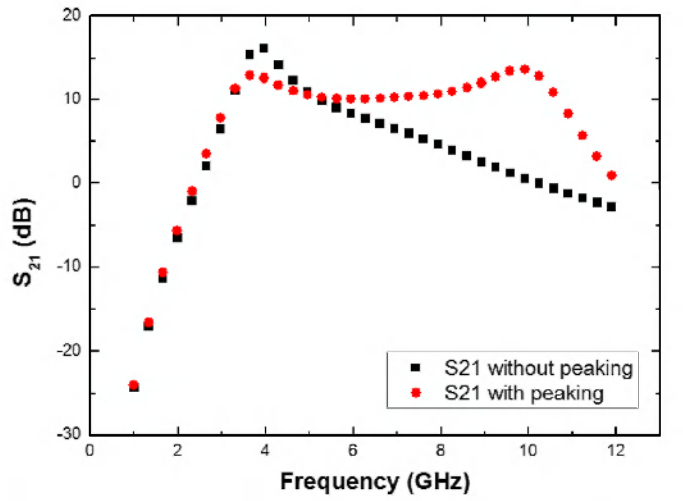

Fig. 8. Calculated frequency responses of voltage gain (*S*21) versus frequency compared to that without series-inductor peaking.

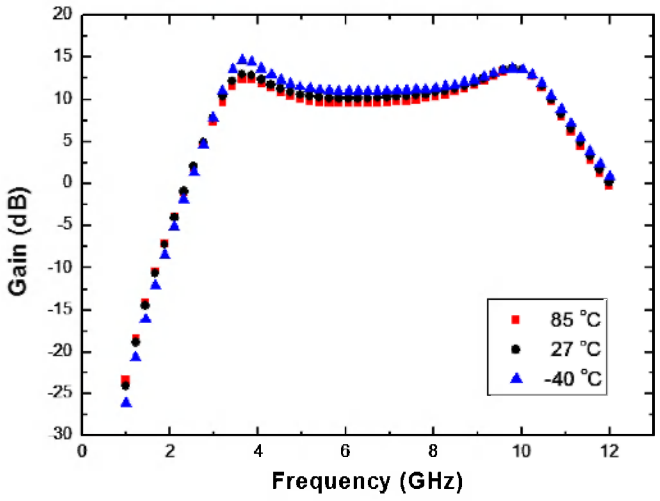

Fig. 9. Power gain of LNA versus frequency at different temperatures (Celsius).

2.3. *Current-reused and stagger tuning technique*

Conventionally, M_1 and M_2 are connected as a cascade topology to design a noise-canceled UWB LNA [7–10]. There are common-gate stage (M_1), which provides wide input impedance matching for the wideband and the cascode stage (M_2 and M_3 with W/L= 60/0.18 μm), which provides the gain over the entire band. To save power consumption, the current-reused technique was employed in Fig. 1. M_2 was stacked on the top of M_1. When the drain current is passed, M_1 and M_2 are regarded as a cascode topology, which consumes the same current to operate each transistor at the same time. Some passive components are needed for the current-reused structure. C_2 is a coupling capacitor, which provides a signal path between the common-gate (M_1) and common-source (M_2) stages. C_b is a bypass capacitor, which blocks the AC signal into the source of M_2 and increase the AC gain of the common-source stage. It functions as an AC ground at high frequency. The capacitance of C_b was chosen to be large as the working AC ground, i.e., 4 pF. L_2 is a RF choke inductor, which prevents the AC signal from passing through using high impedance from the drain of M_1 to the source of M_2. L_2 is the inductor load of the first stage. The values of L_2 with C_b affect gain flatness in the design employing the stagger tuning technique. By controlling the gain peak at the lower bound of the frequency range, a very flat gain curve can be obtained over wide frequency ranges. In addition, the size of transistor, M_1, and the bias condition are also considered for low power consumption. The transistor M_3 is added to mitigate the Miller effect and has a better reverse isolation, thus increasing the stability of the LNA.

The stagger tuning technique has been reported to achieve a flat gain in the wide frequency range [13]. This technique was adopted to achieve a flat gain over the entire band in the proposed UWB LNA. Fig. 5 shows a schematic diagram of the stagger tuning technique. This technique provides inter-stage matching at the low frequency and high frequency bands. The first inter-stage matching resonated at 3 GHz between M_1 and M_2. C_{totl} and L_2 are the main components to provide resonance for designing a flat gain. C_{totl} is the total capacitances including the parasitic and bypass capacitances. Therefore, the low resonance frequency band can be derived as follows:

$$f_{low} = \frac{1}{2\pi}\sqrt{\frac{1}{L_2 C_{totl}}} \tag{7}$$

The second inter-stage matching was provided by L_3 and C_{toth} at 10 GHz. C_{toth} is the total parasitic capacitance at the drain node of transistor, M_3. Therefore, the high resonance frequency can be expressed as follows:

$$f_{high} = \frac{1}{2\pi}\sqrt{\frac{1}{L_3 C_{toth}}} \tag{8}$$

By adopting the current-reused technique in the noise-canceled UWB LNA, it consumes lower power. This LNA core circuit consumes 8.2 mW from a 1.8 V power supply. It also provides a flat gain using the inter-stage matching at the low frequency and high frequency bands.

3. Simulation results of the proposed UWB LNA

The proposed UWB LNA was designed with the TSMC 0.18 μm CMOS RF process using a 1.8 supply voltage. Transistor M_5 acts as a buffer for the measurements. It is connected to transistor M_6, which is a current source for M_5. It dissipates 7 mW with a 1.8 V supply. Therefore, the total power consumption is 15.2 mW. The S-parameters, noise figure and IIP3 were simulated on the schematic-level using a Cadence RF Spectre.

3.1. Gain, return loss and reverse isolation

Fig. 6 shows the input return loss (S_{11}) and gain (S_{21}). S_{11} is below −10 dB from 3.1 GHz to 10.6 GHz. The transconductance of the common-gate stage (M_1) was chosen to be approximately 20 mS for a wide input impedance matching to 50 Ω. L_1 is used to resonate with the parasitic capacitances (C_{gs1} and C_{gs4}) at the center frequency (6.5 GHz). S_{21} is above 10 dB in the entire band. L_2, L_3, C_b and other parasitic capacitances were used to obtain a flat gain over the entire 7.5 GHz bandwidth. The flat gain (10.4–12.6 dB) can be achieved using the inter-stage matching at 3 GHz and 10 GHz. The reverse isolation (S_{12}) is < -23 dB due to RF chock inductor (L_2) and bypass capacitor (C_b) between transistor M_1 and M_2 within the required bandwidth. Fig. 7 shows the simulated K-factor and $B1$-measure of the UWB LNA. The UWB LNA which has the simulated K-factor over unity is unconditionally stable over the band of interest. Theoretically, the K-factor by itself is not sufficient to insure stability, and an additional condition should be satisfied. One such parameter is the stability measure, $B1$, which should be greater than zero. Fig. 8 shows the effect of bandwidth extension using series inductor peaking. The inductor (L_4) reduces the loss from the gate-source parasitic capacitance of M_5 with increasing frequency. Therefore, the gain was increased by approximately 12 dB in the high frequency region. Fig. 9 shows the variation of power gain versus frequency at different temperatures while other parameters are constant. The LNA power gain is robust to temperature variation.

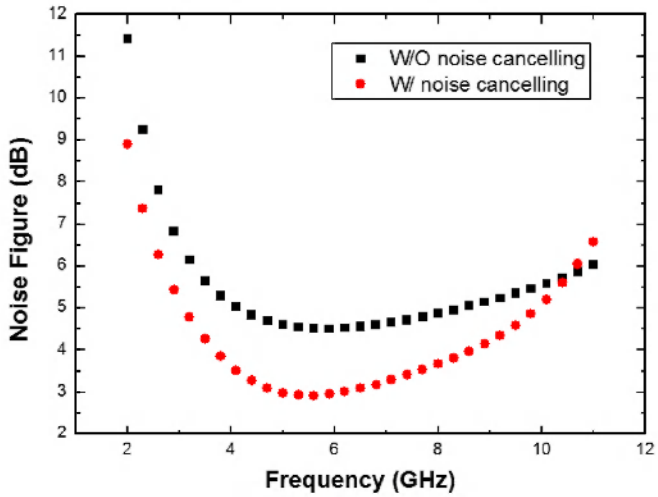

Fig. 10. Simulated noise figure characteristics versus frequency with M_4 and without M_4 for the proposed UWB LNA. The minimum noise figure was 2.9 dB near the zero value in Fig. 4. The maximum noise figure is 5.4 dB.

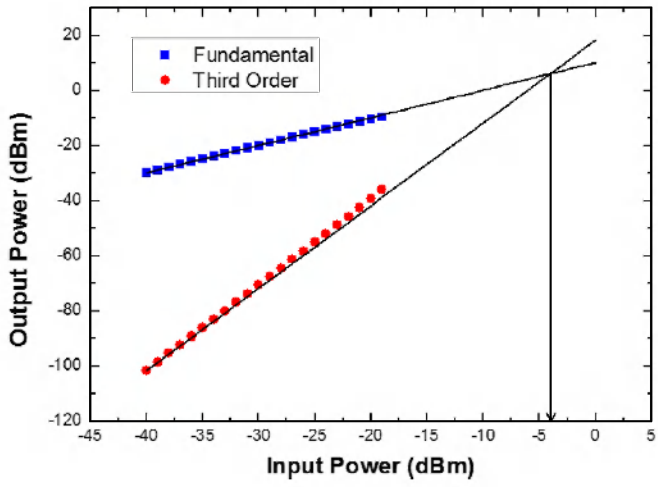

Fig. 11. Simulated results of IIP3 at 6.5 GHz with the two tone test using the 10 MHz spacing. The input power was swept from −40 dBm to 0 dBm.

3.2. Noise figure

Fig. 10 shows the noise figure with and without noise canceling technique of the proposed UWB LNA. The noise figure is within 2.9–5.4 dB over the entire band. The minimum noise figure was checked near 4.8 GHz. This is connected to the noise imbalance simulation result, which has a zero value, as shown in Fig. 4. The maximum noise figure is represented at the high frequency area.

3.3. Linearity

The simulation result also shows the input third-order-intercept points (IIP3). Fig. 11 shows the simulated IIP3 applying two tones with a 10 MHz spacing at 6.5 GHz. The input power was swept from −40 dBm to 0 dBm. The result of IIP3 was −4.62 dBm at 6.5 GHz. Fig. 12 shows the variation of IIP3 versus frequency at different temperatures while other parameters are constant.

Table 1 lists the performance of the proposed noise-canceled UWB LNA along with other previously reported noise-canceled UWB LNAs for comparison. This work provides some advantages, such as high bandwidth, sufficient and flat gain, and lower power consumption.

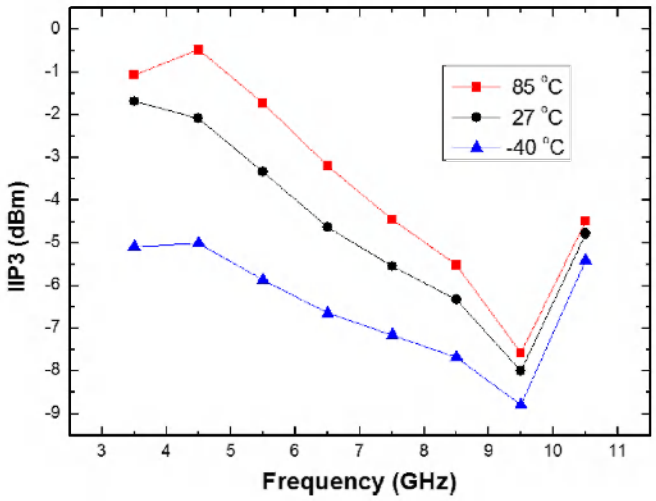

Fig. 12. Variation of IIP3 versus frequency at different temperatures (Celsius).

Table 1
Performance of the proposed UWB LNA and comparison with other noise-canceled UWB LNAs.

	Process (μm)	BW [GHz]	$Gain_{max}$ [dB]	NF [dB]	IIP3 [dBm]	Power (core) [mW]
This work	0.18	3.1–10.6	12.6	2.9–5.4	−4.6	15.2 (8.2)
[3]	0.18	3.1–10.6	17.5	3.1–5.7	–	33.2
[6]	0.18	2–10.6	14.8	4.3–5.5	−6	24 (12)
[7]	0.18	1.2–11.9	11	3.8–5.1	−6.2	29 (20)
[8]	0.13	2.6–12	12	2.8–4.2	−7.2	19

4. Conclusion

A low power noise-canceled UWB LNA was proposed and evaluated for 3.1–10.6 GHz applications using TSMC 0.18 μm RF CMOS technology. The proposed UWB LNA was designed using the noise canceling technique and with the current-reused technique to improve the power dissipation, which generates common-gate and common-source stages using the same DC bias current. The noise canceling topology reduces the dominant noise source using the fully correlated noise voltage, which is provided by the common-gate transistor (M_1). Stagger-tuning was also employed in the proposed circuit to achieve a sufficient and flat gain by adopting inter-stage matching in a desired frequency band. From 3.1 to 10.6 GHz, the gain was 10.4–12.6 dB and $S_{11} < -10$ dB. The noise figure was 2.9–5.4 dB. The total power was 15.2 mW including the output buffer with a 1.8 V power supply.

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